

Design Rules Verification Report

Filename : H:\Projects\Signetik\Signetik-DEV-A1\trunk\cellular-breakout-adapter\interface.Pct

Warnings 0
Rule Violations 0

Warnings	
Total	0

Rule Violations	
Clearance Constraint (Gap=7mil) (All),(All)	0
Short-Circuit Constraint (Allowed=No) (All),(All)	0
Un-Routed Net Constraint ((All))	0
Modified Polygon (Allow modified: No), (Allow shelved: No)	0
Width Constraint (Min=99999mil) (Max=50mil) (Preferred=10mil) (All)	0
Power Plane Connect Rule(Relief Connect)(Expansion=20mil) (Conductor Width=10mil) (Air Gap=10mil) (Entries=4)	0
Hole Size Constraint (Min=1mil) (Max=200mil) (All)	0
Hole To Hole Clearance (Gap=10mil) (All),(All)	0
Minimum Solder Mask Sliver (Gap=10mil) (Disabled)(All),(All)	0
Silk To Solder Mask (Clearance=10mil) (Disabled)(IsPad),(All)	0
Silk to Silk (Clearance=10mil) (Disabled)(All),(All)	0
Net Antennae (Tolerance=0mil) (All)	0
Room Interface (Bounding Region = (7045mil, 1060mil, 8070mil, 1365mil) (InComponentClass('Interface'))	0
Height Constraint (Min=0mil) (Max=1000mil) (Preferred=500mil) (All)	0
Total	0